EE 434
Homework Assignment 2
Fall 2006

Problem 1 Determine the cost per good die for a die that is 5000u x 5000u in a process where 8 inch wafers cost $950 if the defect density is 1.5/cm^2

Problem 2 A mask shrink is often used to decrease die area and increase performance. A die shrink involves simply making a small scaling of all lateral dimensions without doing a re-design of the circuit. How would the cost per good die for the circuit considered in Problem 1 change if the same process were used but there was a 10% die shrink. Are the changes in cost significant?

Problem 3 A circuit has 10 operational amplifiers that all must have an offset voltage of less than 8mV for the circuit to meet parametric requirements. If the standard deviation of the offset voltage is 4mV, determine the soft yield of this integrated circuit as determined by the offset voltages of the op amps. Assume the offset voltages of the 10 operational amplifiers are uncorrelated.

Problem 4 1.3 of Weste and Harris (WH)

Problem 5 1.4b of WH

Problem 6 1.5c of WH

Problem 7 In class we discussed a factor of 10x overhead or more for the total area per transistor relative to the gate area per transistor to allow for spacing between devices and interconnections. The author suggests the overhead factor is somewhat larger. What overhead factor is suggested by the author for random logic.

Problem 8 Estimate the area required for the 4-input NOR gate of Problem 4 in the circuit is designed in a 0.5u CMOS process using the overhead estimates of Sec. 1.10.5.

Problem 9 The input impedance to a scope can be modeled with the parallel combination of a resistor R_S and a capacitor C_S as depicted below. A 10x scope probe is to provide an attenuation of 10 for all input frequencies. Give the value of the probe impedance, R_P, and the probe capacitance C_P, that will provide this attenuation and show that the attenuation of the probe is independent of frequency if these probe impedances are used.